REMARKS

This Amendment is accompanied by a Petition for a Three-Month Extension of Time, and the related extension fee.

Within the Office Action, the Examiner indicated that claims 19 and 33 would be considered allowable if rewritten in independent form including the limitations of the base claim and any intervening claims. Claim 19 has been rewritten in independent form to include the limitations of claims 12, 14 and 18. Similarly, claim 33 has been rewritten in independent form to include the limitations of claims 26, 29 and 32. In the process of amending claim 19, Applicant's attorney noted that claim 19 inadvertently duplicated certain elements of the "delay locked loop adjustment circuit". For example, within claim 19 as filed, the third line of such claim defined a "calibration pulse generator"; however, later in claim 19, sub-paragraph "a." again lists a calibration pulse generator. The same is true for the other elements of the "delay locked loop adjustment circuit". Accordingly, in amending claim 19, Applicant has eliminated the unintended duplication of such elements. The elements of the "delay locked loop adjustment circuit" retained in claim 19 as amended correspond to such elements as originally set forth in claim 33 as amended. In view of such amendments and the foregoing remarks, Applicant submits that claims 19 and 33 are in allowable form.

Within the Office Action, the Examiner rejected claims 15-17 and 22 under 35 U.S.C. §112, second paragraph, as being indefinite. Applicant has amended claim 15 to clarify its meaning. As amended, claim 15 recites that the display line driver circuit of base claim 12 further includes a plurality of column line driver group circuits each coupled to at least one of said signal taps and wherein each column line driver group circuit has a plurality of column signal lines associated therewith. For example, in Fig. 5 of Applicant's patent drawings, CD1 (70), CD2 (72), CD3 (74), and CD4 (76) form a plurality of column line driver group circuits, each of which is coupled to a signal tap along the delay line formed by the R-C network that includes resistors 66 and capacitors 68. Further, as shown best in Fig. 9, each such column line driver group circuit has a plurality of column signal lines C_1, C_2 . . . C_M associated therewith.

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Applicant respectfully submits that the amendments made above to claim 15 eliminate any indefiniteness which may have previously existed in such claim, and that claim 15 (and claims 16, 17 and 22 which depend therefrom) now comply with 35 U.S.C. §112, second paragraph.

Within the Office Action, the Examiner also rejected claims 1-12, 15, 22-26, 29 and 36-40 under 35 U.S.C. §102(e) as describing subject matter considered to be anticipated by U.S. Patent No. 6,628,273 to Rindal, et al. (hereinafter, "Rindal"). However, as will be explained below, Rindal fails to disclose all of the features recited by such claims.

Claim 1 recites a method of operating an LCD display including pixels arranged in an array of rows and columns; claim 1 further recites that the LCD display includes row driver circuitry having a row driver for each row of the array, and column driver circuitry having a column driver for each column of the array. In addition, claim 1 recites that the row driver circuitry applies a row enable signal to a selected one of the row conductors to enable the pixels within the selected row; claim 1 also explains that the column driver circuitry drives voltages onto the columns of the LCD display for storage in the pixels of the selected row. This type of addressing scheme is known to those skilled in the art as an active matrix LCD display.

However, this is not how the cited Rindal disclosure functions. Rindal notes, in describing his drawing labeled "FIG. 1 (PRIOR ART)", that it is known in the art to employ separate row drivers (R1, R2, R3, ... RN) for every row in the pixel matrix, and separate column drivers (C1, C2, C3, C4, ... CM) for every column in the pixel matrix. In contrast, Rindal's stated goal is to reduce the number of drivers needed to address the pixels in the display; see Rindal specification, col. 2, lines 19-49. Rindal achieves this goal by substituting a single column driver 210c and a single row driver 210r (shown in Rindal's Fig. 2) in place of the multiple row drivers (R1, R2, R3 ...RN) and multiple column drivers (C1, C2, C3, C4,... CM) shown in Rindal's "Prior Art" Fig. 1. Thus, instead of the active matrix display scheme shown in Rindal's "Prior Art" Fig. 1, Rindal substitutes a so-called "passive matrix display" wherein only one pixel is written at a time, and wherein the voltage to be applied across each pixel is the differential voltage across the row line and column line to which such pixel is coupled. Rindal

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explains that voltage V1 is applied to column conductor 240c, and that voltage V2 is applied to row conductor 240r; each pixel in Rindal's array is either turned on or turned off based upon the differential voltage V2-V1 applied across the pixel by the row line and the column line; see Rindal specification, col. 6, lines 34-45. It is not possible, within the passive matrix display of Rindal to enable a particular row of pixels all at once, and to then apply desired voltages to the individual column driver lines of the display. Rather, in Rindal, the voltage V2 on the row conductor 240r must be adjusted for each pixel in the selected row depending upon the value of the data to be written in such pixel.

As amended, claim 1 recites that a row enable signal is applied to a first selected row conductor of the LCD display via the row driver circuitry at a first predetermined time and for a predetermined duration; for example, in Fig. 2 of the present application, row enable signal 20 has a pulse width indicated by the dashed lines designating the rising and falling edges of the row enable signal. Claim 1 further recites that the first column driver is enabled for applying a first driving voltage onto the first column of the LCD display at a second predetermined time and during said first predetermined duration to transfer a first driving voltage onto a first pixel; claim 1 also recites that the second column driver is enabled at a third predetermined time and during said first predetermined duration to transfer a second driving voltage onto a second pixel. Moreover, amended claim 1 states that the third predetermined time is delayed beyond the second predetermined time by a delay that is approximately equal to the propagation delay of the row enable signal along the selected row conductor but less than said first predetermined duration. In other words, at least two pixels in an enabled row are driven during the predetermined duration of the same row enable signal.

In contrast, in Rindal, each row "enable" signal (drive pulse) driven onto row conductor 240r causes, at most, only one pixel to be driven. In regard to Figs. 5 and 6 of Rindal, the positive-going pulse in waveform 281 has a predetermined duration, but during such predetermined duration, only one pixel (pixel A of Fig. 5) can be updated. During subsequent pulses, the rest of the pixels can be successively updated. Thus, Rindal teaches that only one pixel is updated over the duration of each row enable signal; in this regard, Rindal notes that

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pixel A is updated, if at all, during time interval 286, and that the other pixels of the display must be sequentially addressed during respective subsequent intervals designated as period 287; see Rindal, col. 6, lines 46-67. This is the cost paid by Rindal for reducing the number of separate column drivers from M (where M is the number of columns in the array - see Fig. 1 of Rindal) to one.

Given the foregoing distinctions between claim 1 as amended and the cited Rindal patent, Applicant respectfully submits that Rindal neither anticipates nor suggests the invention defined by claim 1.

Claim 3 defines a method of operating an LCD display including pixels arranged in an array of rows and columns, the LCD display again including row driver circuitry having a row driver for each row of the array for applying a row enable signal to a selected one of the rows to enable the pixels within the selected row. Method claim 3 also recites that the LCD display includes column driver circuitry having a column driver for each column of the array for driving voltages onto the columns of the display for storage in the pixels of the selected row. The method of claim 3 further includes the steps of enabling a row driver for applying the row enable signal to a second row located relatively distant from the column driver circuitry for a predetermined duration, and storing the driving voltages driven onto the columns of the LCD display into each of the pixels of the enabled second row during such predetermined duration.

Once again, Rindal does not identically disclose, nor suggest, such a method of operating an LCD display. Rindal does not provide separate row drivers for each row of the array, does not provide separate column drivers for each column of the array, and does not enable a selected row for a predetermined duration during which all of the pixels of the selected row are driven. Rather, in Rindal, each pixel must be sequentially addressed.

Likewise, claim 4 as amended requires a row driver for each row of the array and a column driver for each column of the array, and further requires that each of the pixels in a selected row of the display be addressed during the predetermined duration during which the selected row is enabled. However, this is precisely what Rindal wishes to avoid; Rindal desires to address the display elements sequentially, one-by-one, to avoid the need for a large number of

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row drivers and column drivers.

Similarly, claim 12 recites a display line driver circuit having "a plurality of row drivers corresponding to the number of rows in the array, and ... a plurality of column drivers corresponding to the number of columns in the array". Furthermore, claim 12 recites that each display element is addressed by applying a row enable signal for a predetermined duration to the row in which such display element lies, and that a plurality of the display elements in the selected row are addressed during the predetermined duration of the row enable signal. As noted above, Rindal provides a contrary teaching.

The display driver of claim 26 as amended requires "row driver circuitry including a row driver for each row of the array, ... and column driver circuitry including a column driver for each column of the array". This is once more contrary to the teachings of Rindal.

Claim 38 as amended recites a display signal timing controller for a display having a plurality of display elements arranged in an array of rows and columns, wherein the controller includes a delay locked loop circuit including a plurality of delay elements coupled in series for delaying a first display timing signal, a plurality of taps coupled between select delay elements of the delay locked loop circuit for tapping delayed portions of the first display timing signal; and

output circuitry configured to generate a second display timing signal in response to the first display timing signal. Claim 38 recites that such output circuitry is responsive to the first display timing signal and to the tapped delayed portions of the first display timing signal, and that the second display timing signal changes state in response to the receipt of the first display timing signal and maintains the second display timing signal in such state at least until all of the tapped delayed portions of the first display timing signal have been received. The preferred embodiment of such controller is shown in Fig. 7 wherein phase locked loop 120 includes delay elements, taps (Δ_0, Δ_1, Δ_2 . . . Δ_N), receives a first display timing signal ("IN") and generates a second timing signal ("START"). Neither Rindal nor secondary reference Hush (U.S. Patent No. 5,854,615) disclose or suggest such a timing controller for a display.

Finally, claim 40 again recites a display having row driver circuitry that includes a row

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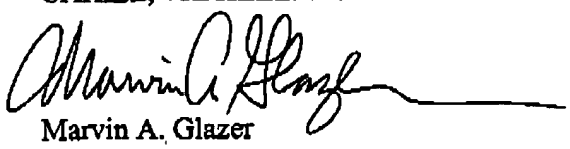
driver for each row of the array, and column driver circuitry that includes a column driver for each column of the array. Claim 40 also requires a ("second") row located relatively distant from the column driver circuitry, and recites that voltages driven onto the columns of the array reach such second row in the same cycle. Once again, this is not the structure taught by Rindal.

In view of the foregoing remarks, and in light of the amendments to the claims, Applicant respectfully submits that the pending claims are patentably distinguishable from the cited art of record, and that the present application is now in condition for allowance, which action is earnestly requested.

Respectfully submitted,

CAHILL, von HELLENS & GLAZER P.L.C.



Marvin A. Glazer
Registration No. 28,801

155 Park One
2141 East Highland Avenue
Phoenix, Arizona 85016
Ph. (602) 956-7000
Fax (602) 495-9475

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